AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A processor comprising:

a scheduler to schedule execution of at least one instruction having at least one source location and a destination location as operands, ~~each~~ the source location and the destination location each ~~comprising~~ including a validity bit; ~~to indicate validity of data in the at least one source location; and~~

an execution unit to execute the instruction; and

a data validity circuit coupled to the ~~at least one source location~~ execution unit to determine the validity of ~~the~~ data in the ~~at least one~~ source location, ~~said~~ the data validity circuit to ~~indicate the validity of the data, by writing a~~ write the validity bit in ~~a~~ the destination location based upon the validity bit in the ~~at least one~~ source data storage location, wherein the scheduler re-schedules execution of the instruction if the value of the validity bit of the destination location indicates invalid data.

2. (Original) The processor of claim 1 wherein writing a validity bit in a destination location comprises writing a bit in a destination register in the processor to indicate validity of data in the destination location.

3. (Currently Amended) The processor of claim ~~2~~ 1, wherein the data validity circuit further ~~comprising~~ comprises a checker unit, the checker unit to retire an instruction having the destination data storage location as an operand according to the value of a validity bit. ~~coupled to the destination location and to an execution unit.~~

4. (Cancelled)

5. (Currently Amended) The processor of claim ~~3~~ 1 wherein the ~~checker unit~~ scheduler re-schedules instructions for re-execution by the execution unit, beginning with the oldest instruction ready instruction.

6. (Original) The processor of claim 3 further comprising a retirement unit coupled to the checker unit to receive instructions that execute with valid data in the destination location.

7. (Original) The processor of claim 1, wherein the data validity circuit comprises any one of an AND-gate and an OR-gate.

8. (Currently Amended) The processor of claim 1 wherein the source data storage location is any one of a register in the processor, cache, and permanent memory, said register, cache and permanent memory having a bit to indicate validity of data in the register, cache, and the permanent memory.

9. (Currently Amended) The processor of claim 1 wherein the destination data storage location is any one of a register in the processor, cache, and permanent memory, said register, cache, and permanent memory having a bit to indicate validity of data in the register, cache, and the permanent memory.

10. (Currently Amended) An method comprising:

writing a bit in one or more source locations of an instruction scheduled for execution, said bit to indicate the validity of the data in each of the one or more source locations;

reading the bit to determine the validity of the data in the one or more source locations;

writing a bit in a destination location of the instruction, said bit to determine the validity of the data in the destination location based on the validity of the bit in the ~~one or more~~ source location; and

re-scheduling ~~an~~ the instruction for execution if the bit in the destination location indicates invalid data.

11. (Original) The method of claim 10 further comprising retiring the instruction if the bit in the destination location indicates valid data.

12. (Original) The method of claim 10 wherein reading the bit to determine the validity of the data in the one or more source locations comprise using any one of an OR-gate and an AND-gate to read the bit in the one or more source locations.

13. (Currently Amended) An apparatus comprising:

means for writing a bit in one or more source locations of an instruction scheduled for execution, said bit to indicate the validity of the data in each of the one or more source locations;

means for reading the bit to determine the validity of the data in the one or more source locations;

means for writing a bit in a destination location of the instruction, said bit to determine the validity of the data in the destination location based on the validity of the bits in the one or more source locations; and

means for re-scheduling ~~an~~ the instruction for execution if the bit in the destination location indicates invalid data.

14. (Original) The apparatus of claim 13 further comprising means for retiring the instruction if the bit in the destination location indicates valid data.

15. (Original) The apparatus of claim 13 wherein the means for reading the bit to determine the validity of the data in the one or more source locations comprises using any one of an OR-gate and an AND-gate to read the bit in the one or more source locations.

16. (Currently Amended) A computer system comprising:

a bus;

a memory unit coupled to said bus;

a processor including:

a scheduler to ~~execute an~~ schedule at least one instruction, ~~said processor comprising~~ having at least one source register and a destination register as operands, ~~each~~ the source register and the destination register each comprising a validity bit; ~~to indicate validity of data in the at least one source register; and~~

an execution unit to execute the instruction; and

a data validity circuit coupled to the ~~at least one source register~~ execution unit to determine the validity of the data in the at least one source register, ~~said~~ the data validity circuit to indicate the validity of the data in ~~a~~ the destination register, by writing ~~a~~ the validity bit in the destination register based upon the validity of the data in the at least one source register; wherein the scheduler re-schedules execution of the instruction if the value of the validity bit of the destination data storage location indicates invalid data.

17. (Original) The processor of claim 16 wherein the validity bit is stored contiguous with data bits.

18. (Currently Amended) The processor of claim 16, wherein the data validity circuit further comprising a checker unit coupled to the ~~destination register and to an~~ execution unit, the checker unit to retire the instruction having the destination data storage location as an operand according to the value of a validity bit;~~.~~

19. (Cancelled)

20. (Currently Amended) The processor of claim 18 wherein the ~~checker unit~~ scheduler re-schedules instructions for re-execution by the execution unit beginning with an oldest instruction ready for execution.

21. (Currently Amended) The processor of claim ~~18~~ 16 further comprising a retirement unit coupled to the checker unit to receive instructions that execute with valid data in the destination register.

22. (Original) The apparatus of claim 16, wherein the data validity circuit comprises any one of an AND-gate and an OR-gate.

23. (Currently Amended) An article of manufacture comprising:

a machine-accessible medium including instructions that, when executed by a machine, causes the machine to perform operations comprising

writing a bit in one or more source registers of an instruction scheduled for execution, said bit to indicate the validity of the data in each of the one or more source registers;

reading the bit to determine the validity of the data in the one or more source registers;

writing a bit in a destination register of the instruction to determine the validity of the data in the destination register based on the validity of the bits in the one or more source registers; and

re-scheduling ~~an~~ the instruction for execution if the bit in the destination register indicates invalid data.

24. (Original) The article of manufacture as in claim 23, further comprising instructions for retiring the instruction if the bit in the destination register indicates valid data.

25. (Original) The article of manufacture as in claim 23, wherein instructions for reading the bit to determine the validity of the data in the one or more source registers comprises further instructions for using at least one of an OR-function and an AND-function to examine the bit in the one or more source registers.